

FIG. 1A (Prior Art)

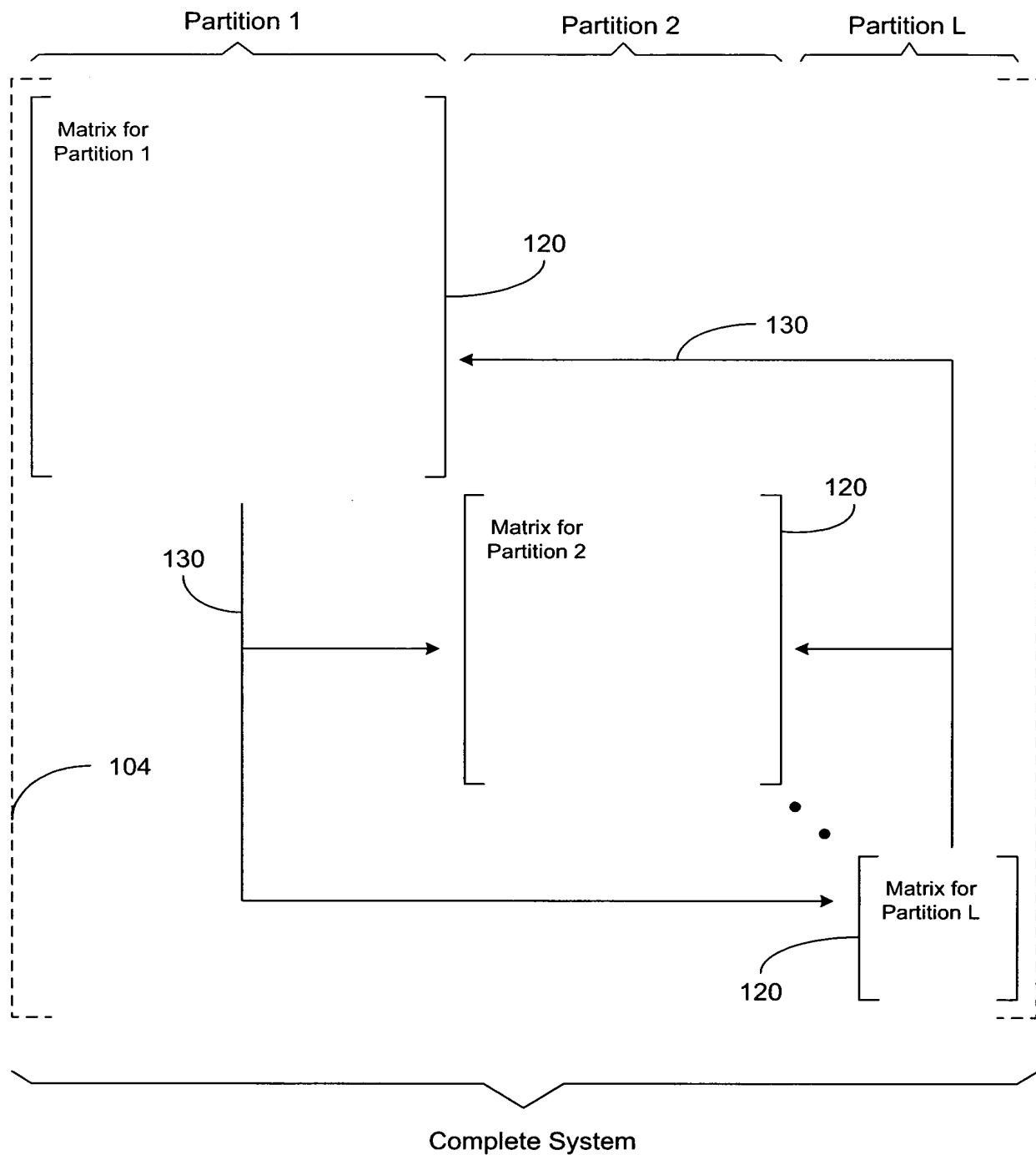


FIG. 1B (Prior Art)

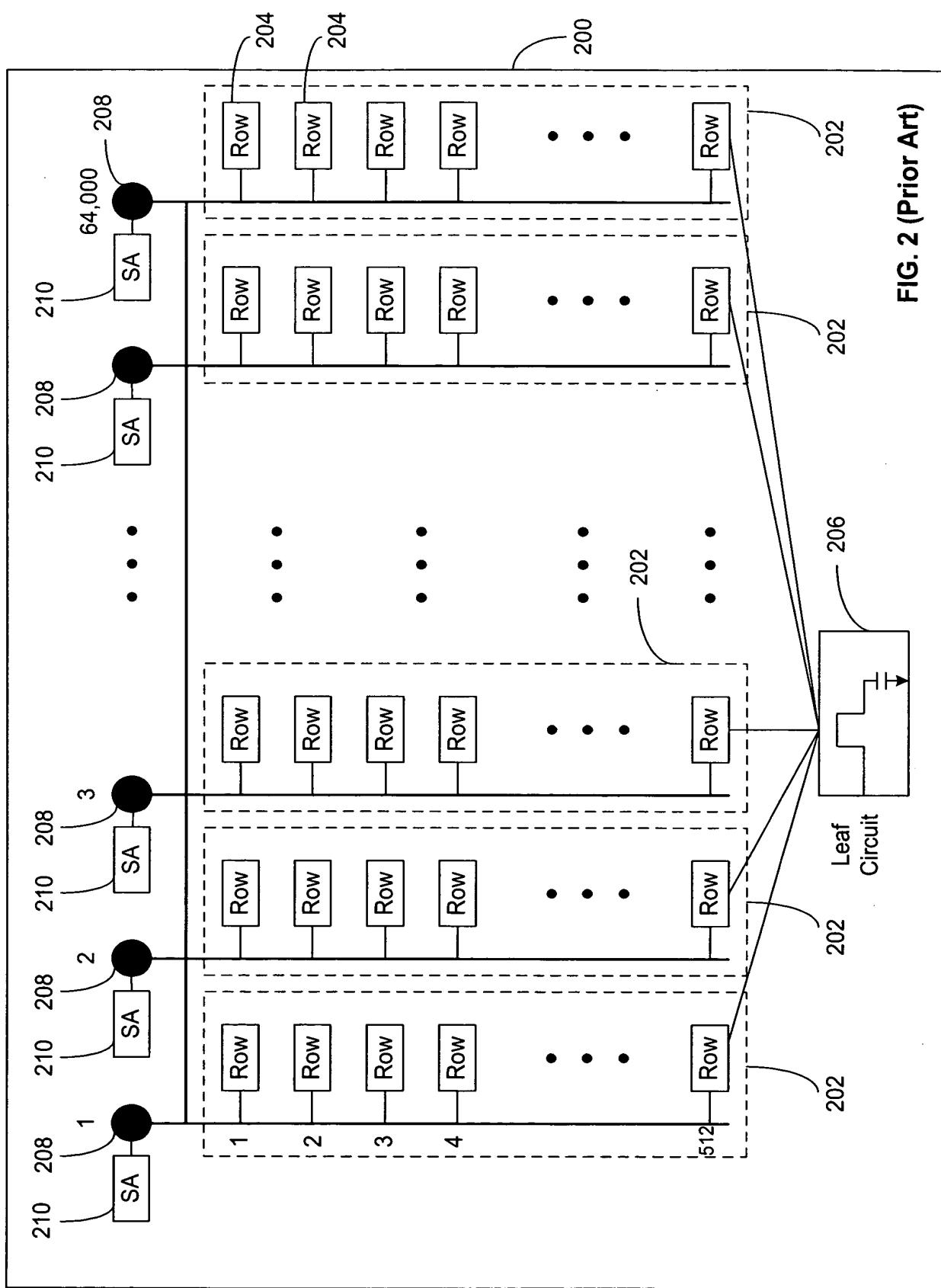


FIG. 2 (Prior Art)

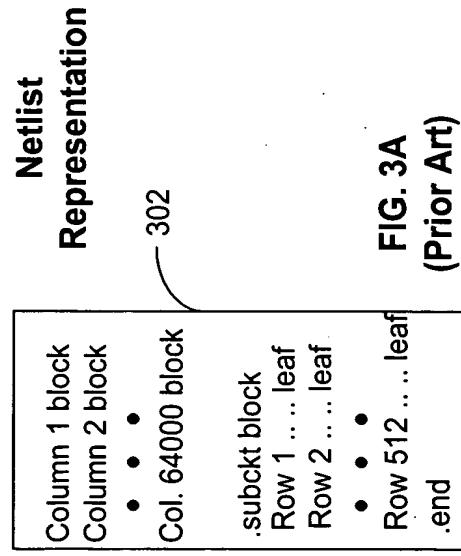


FIG. 3A
(Prior Art)

Physical Representation

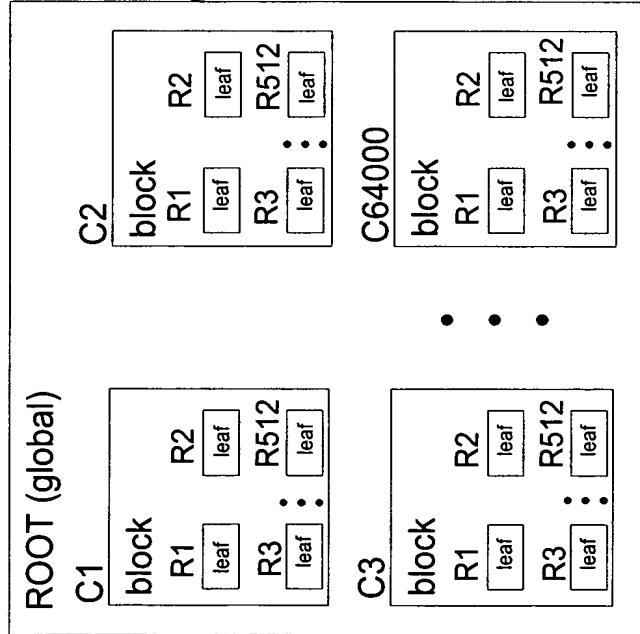


FIG. 3B
(Prior Art)

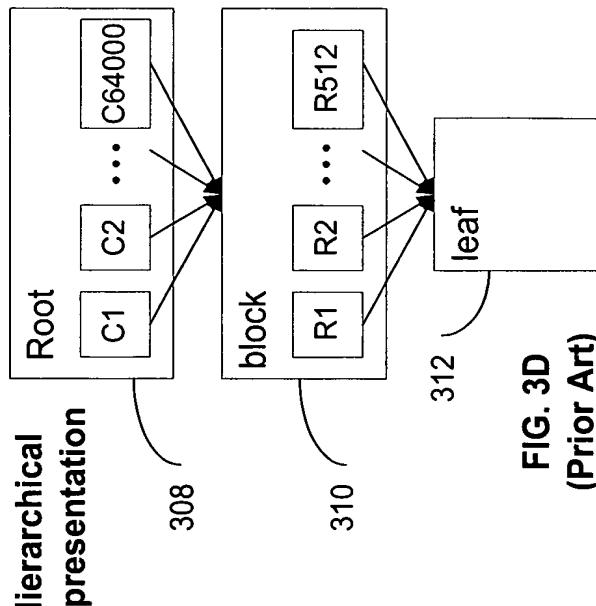


FIG. 3D
(Prior Art)

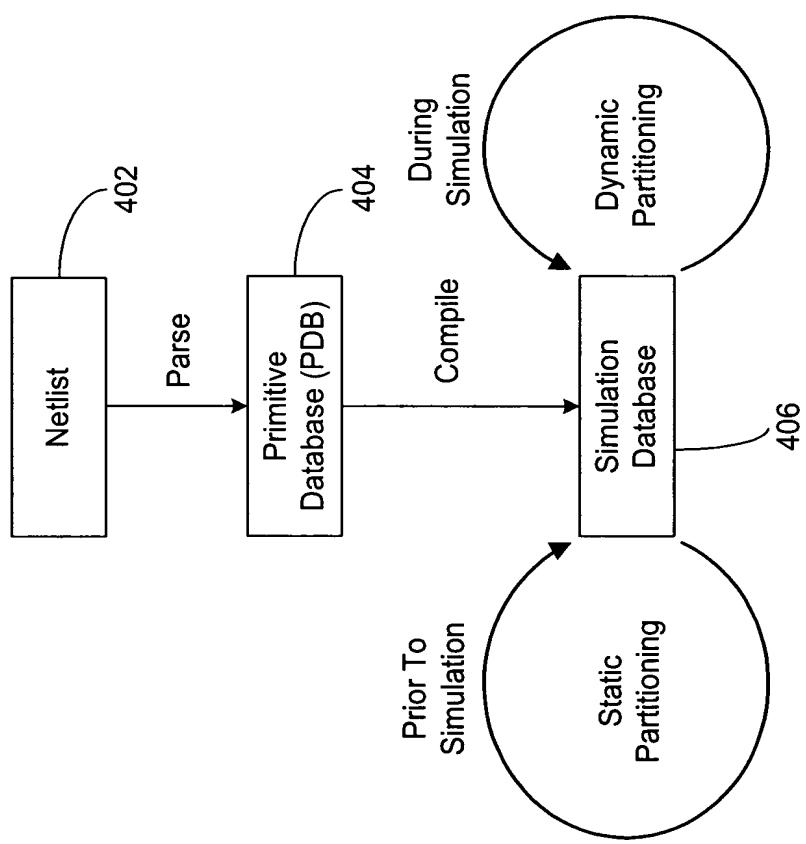


FIG. 4 (Prior Art)

Static Partitioning

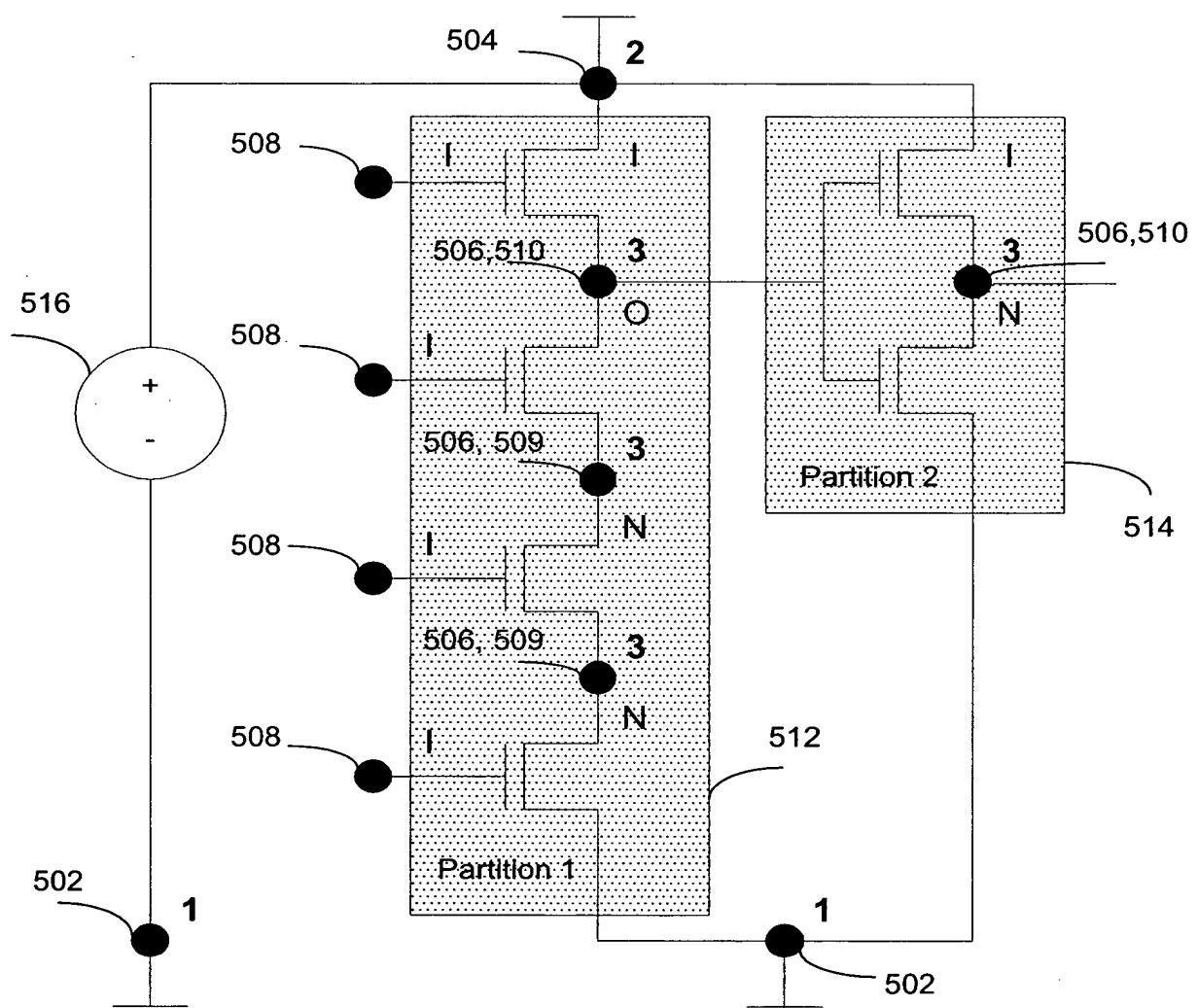


FIG. 5 (Prior Art)

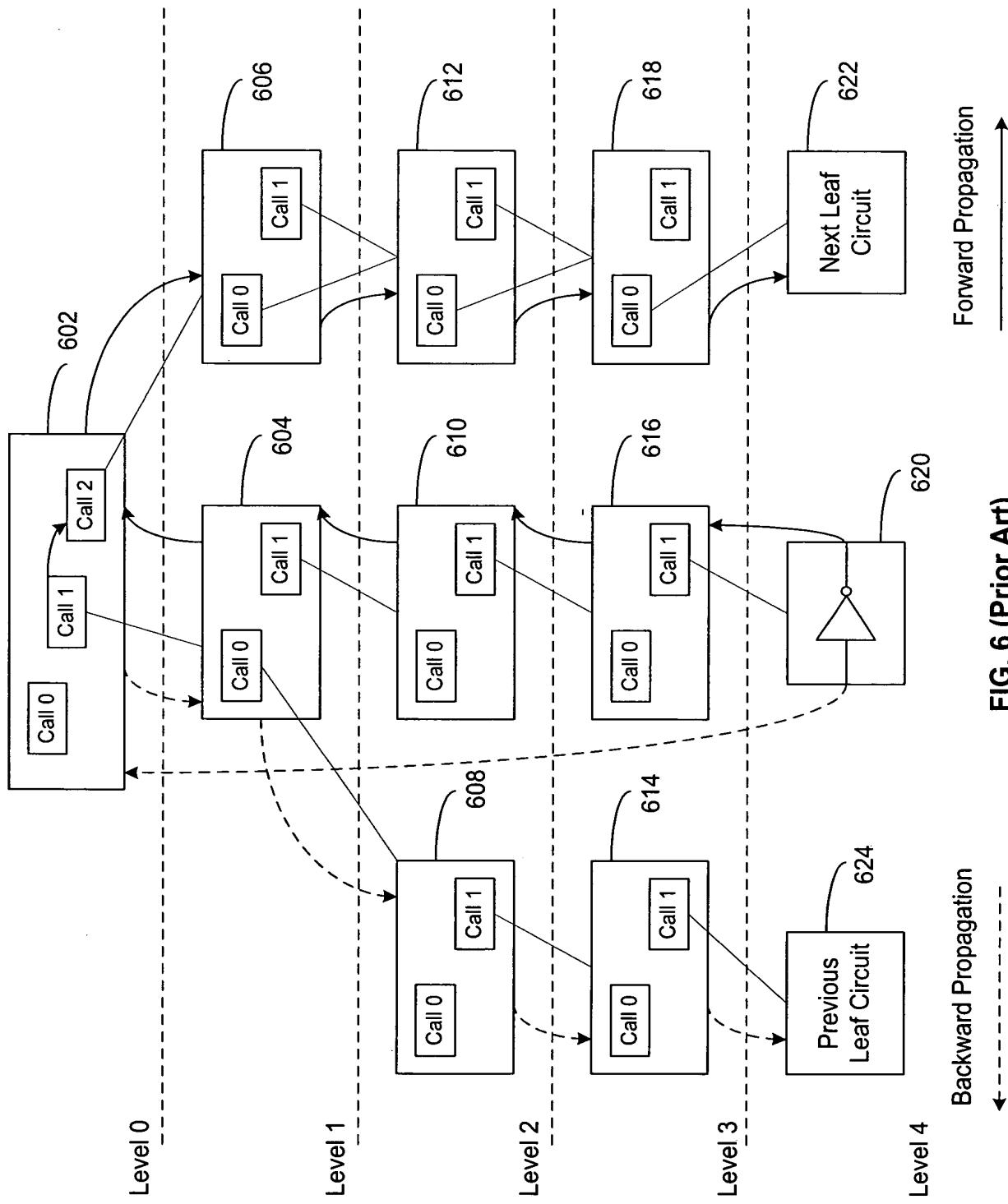


FIG. 6 (Prior Art)

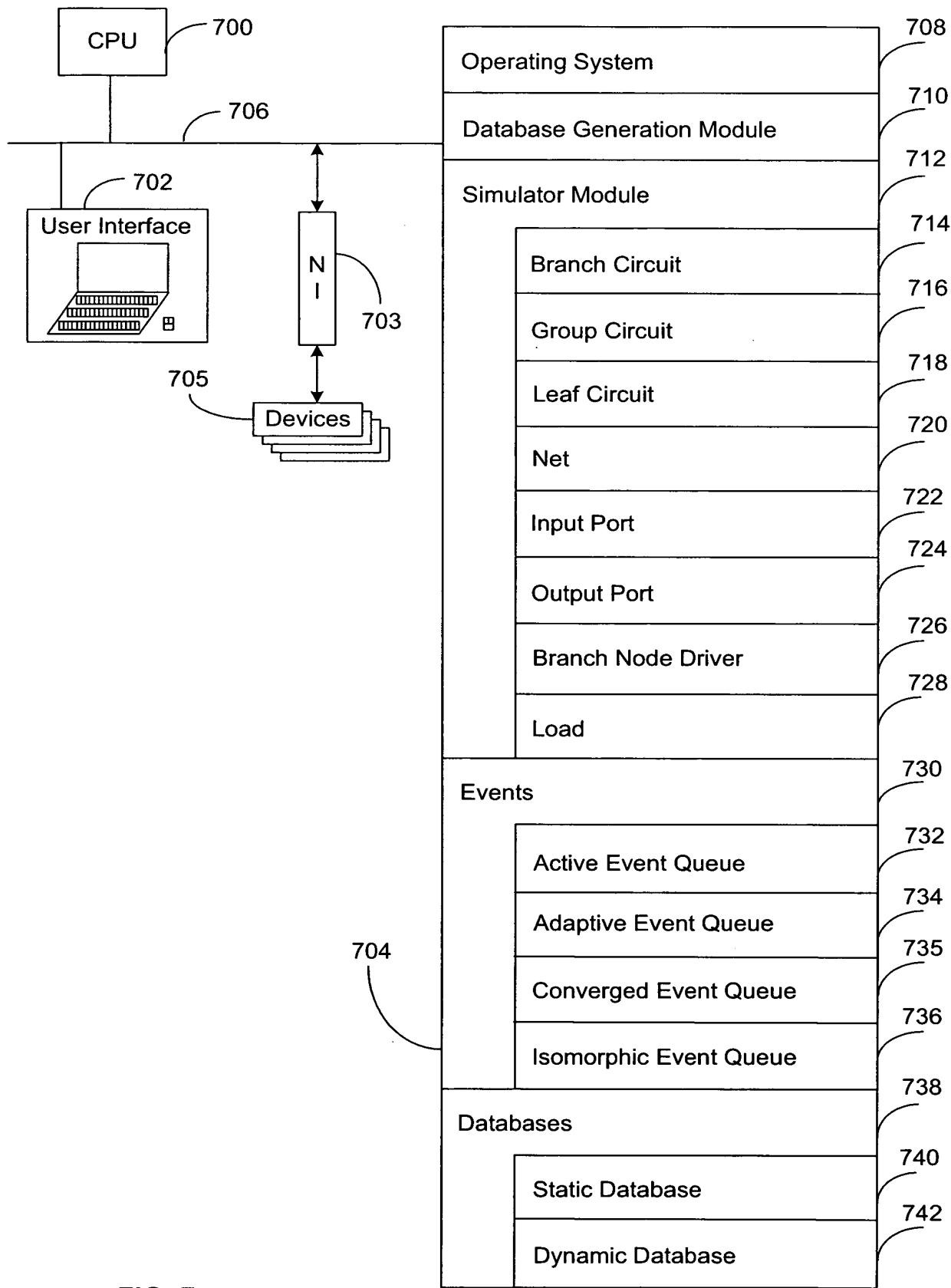


FIG. 7

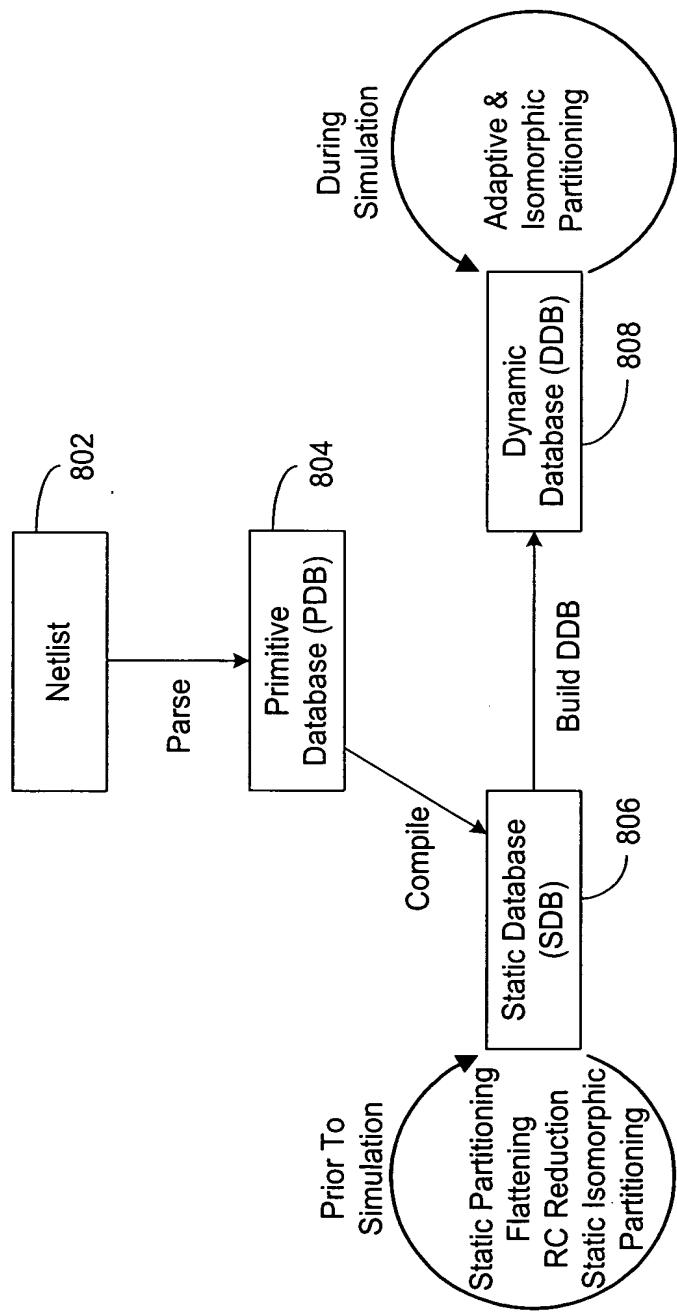


FIG. 8A

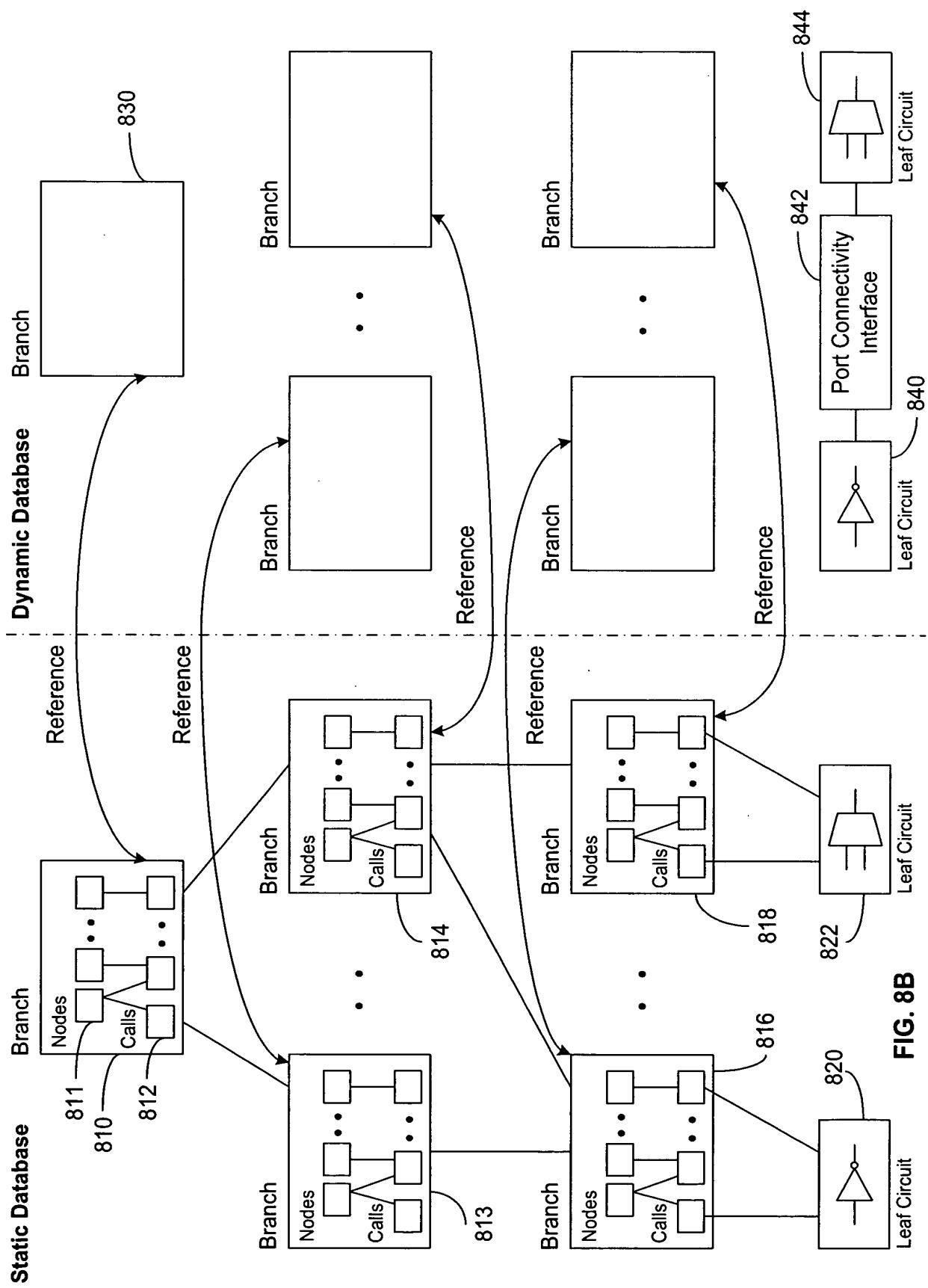


FIG. 8B

Leaf Circuit

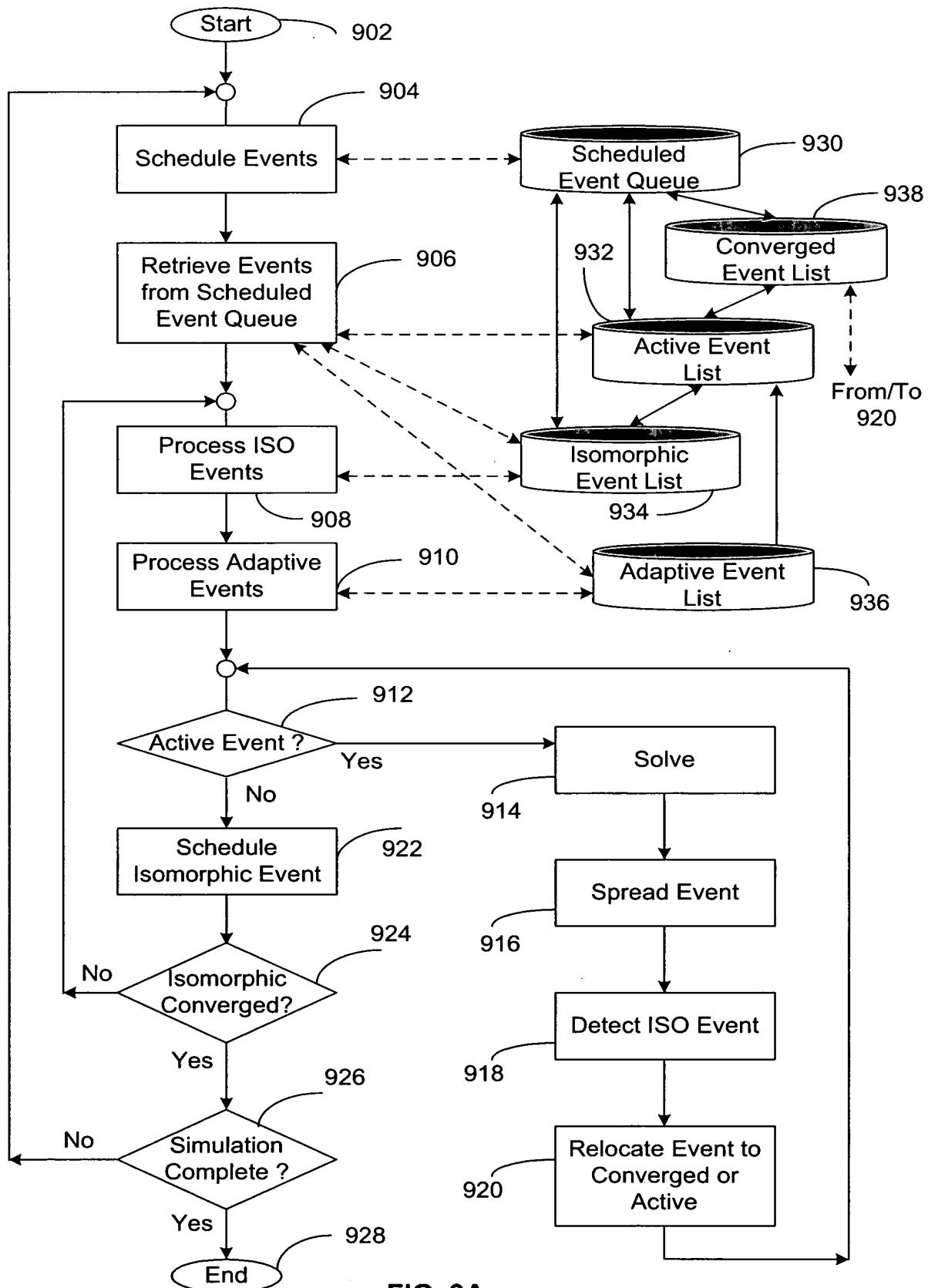


FIG. 9A

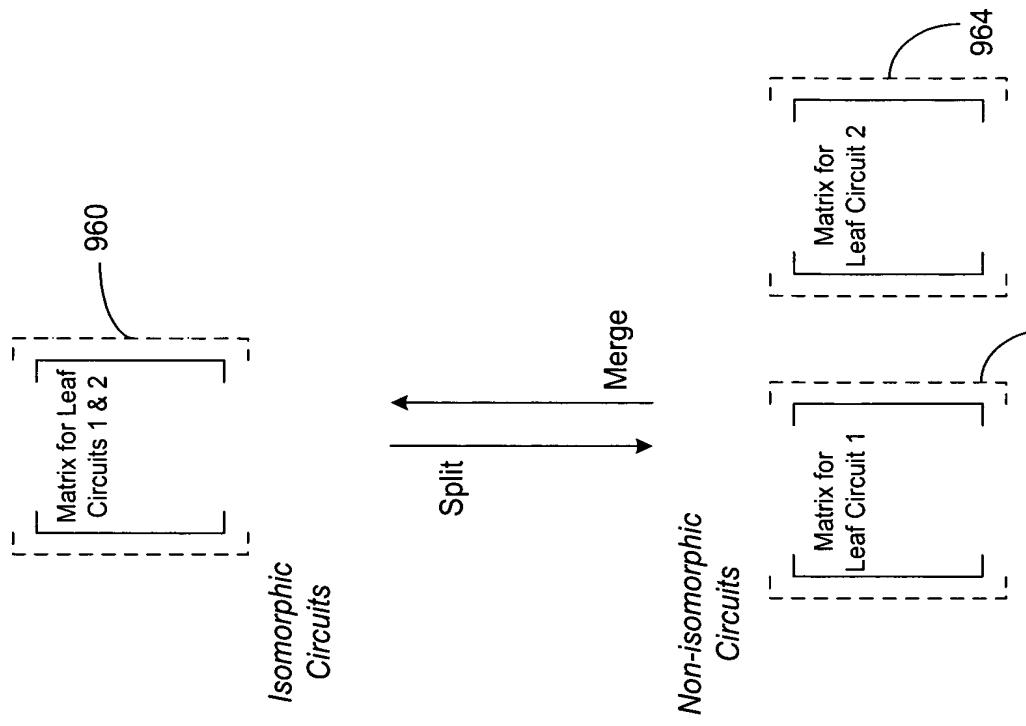
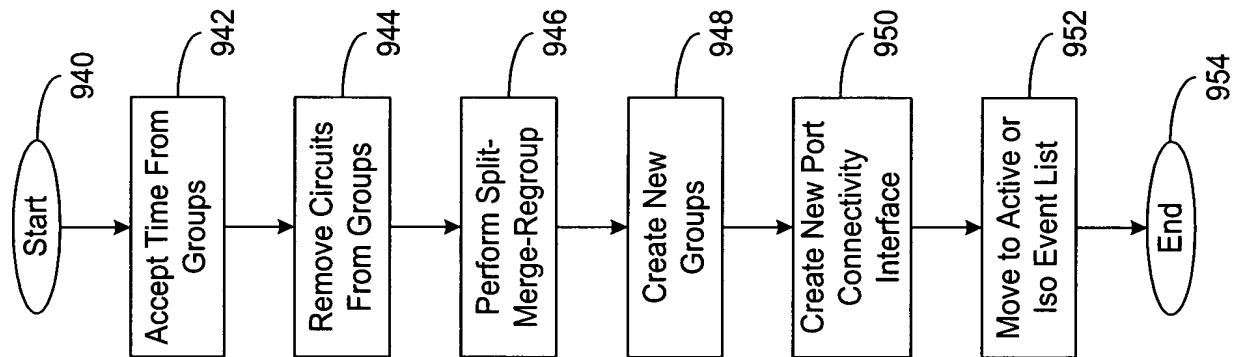


FIG. 9C

FIG. 9B

FIG. 10A

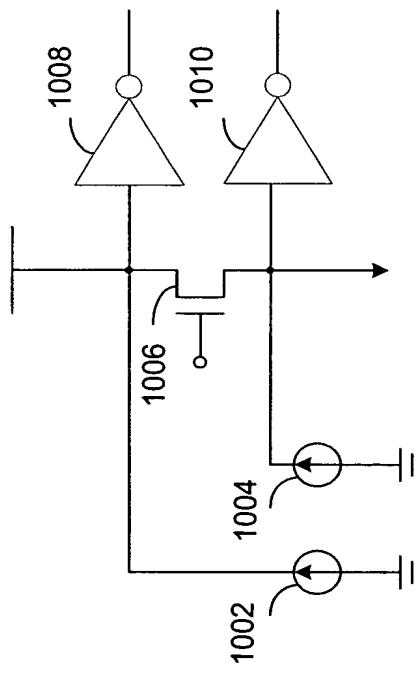
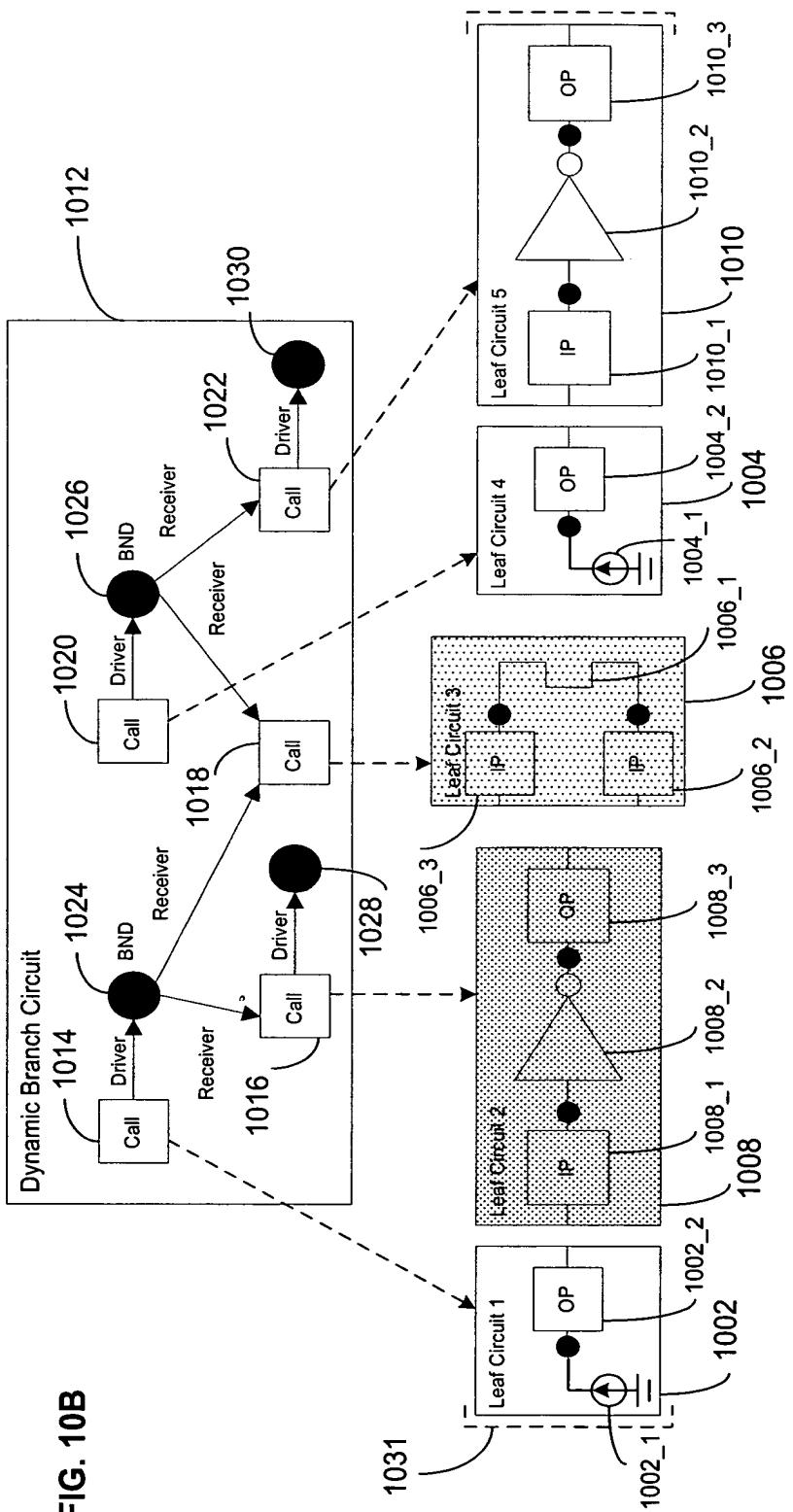


FIG. 10B



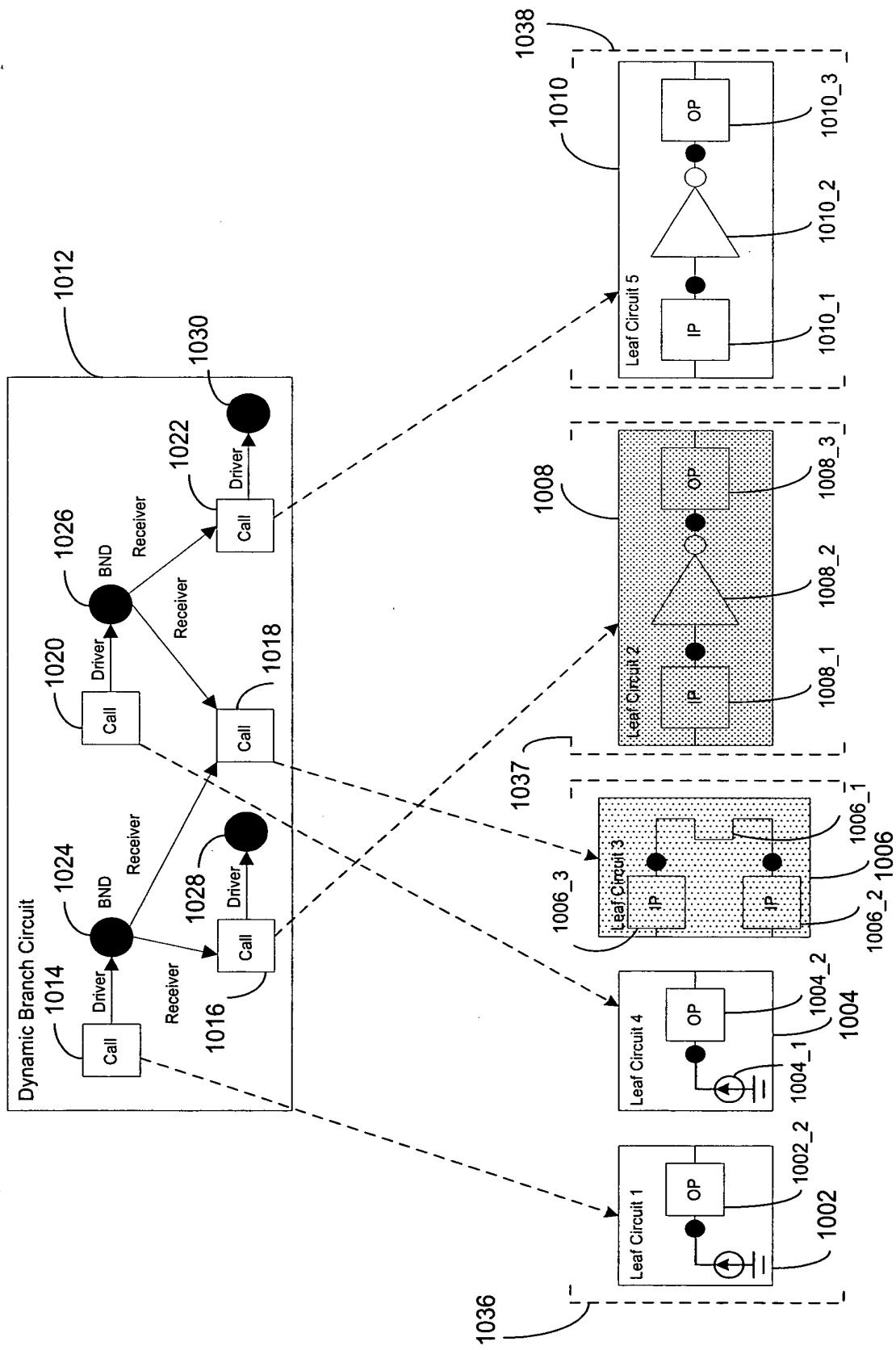


FIG. 10C

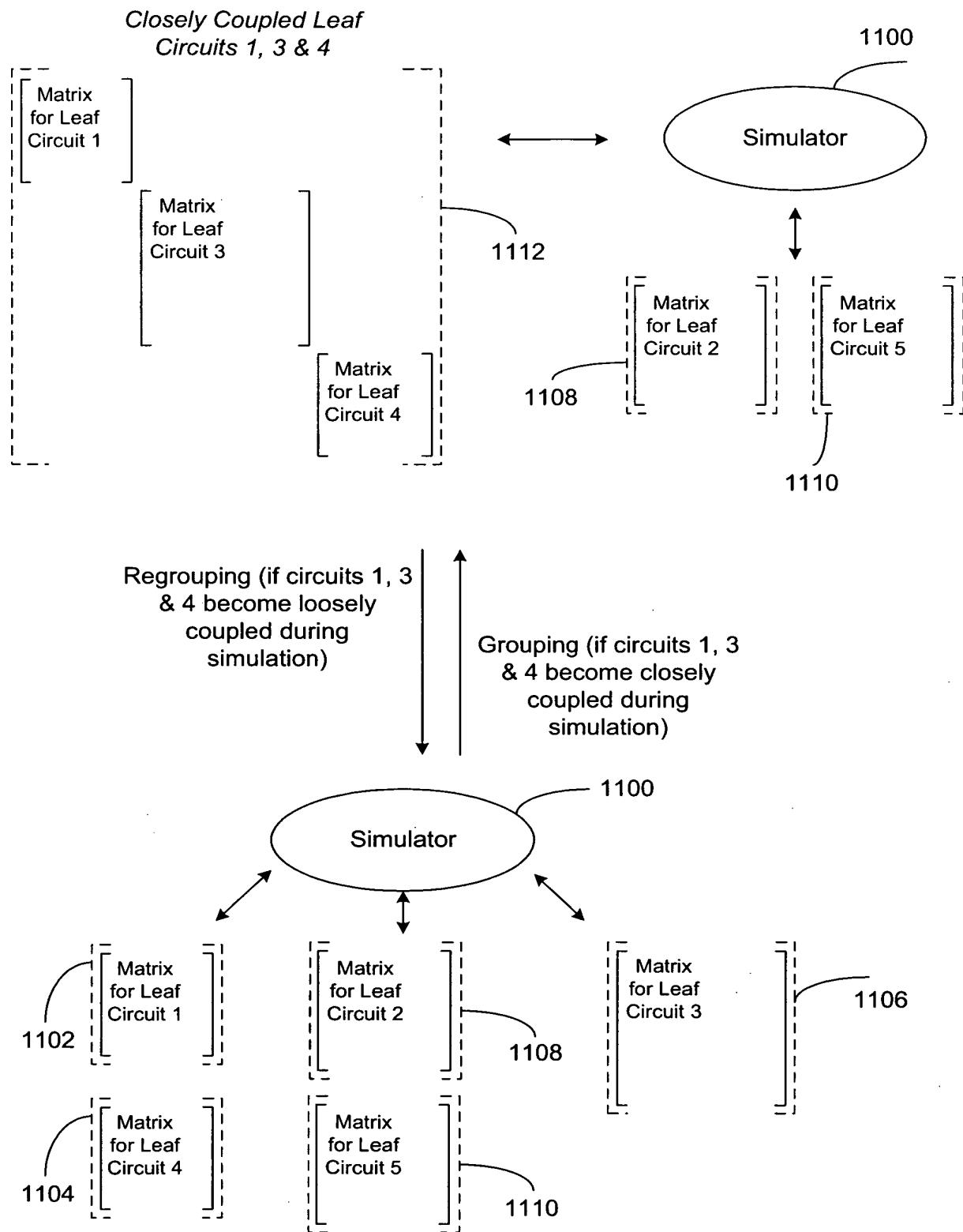


FIG. 11

Loosely Coupled Leaf Circuits

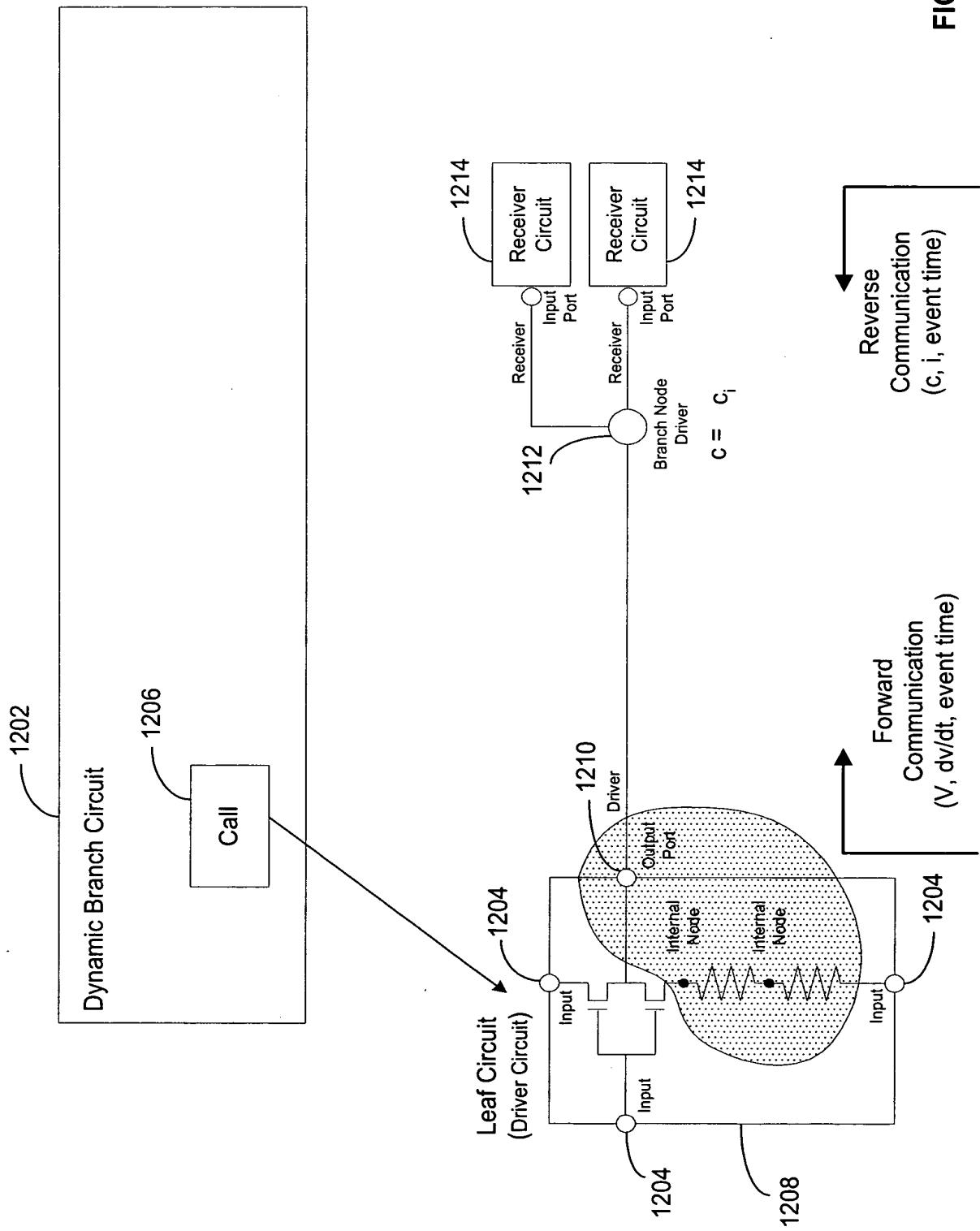


FIG. 12A

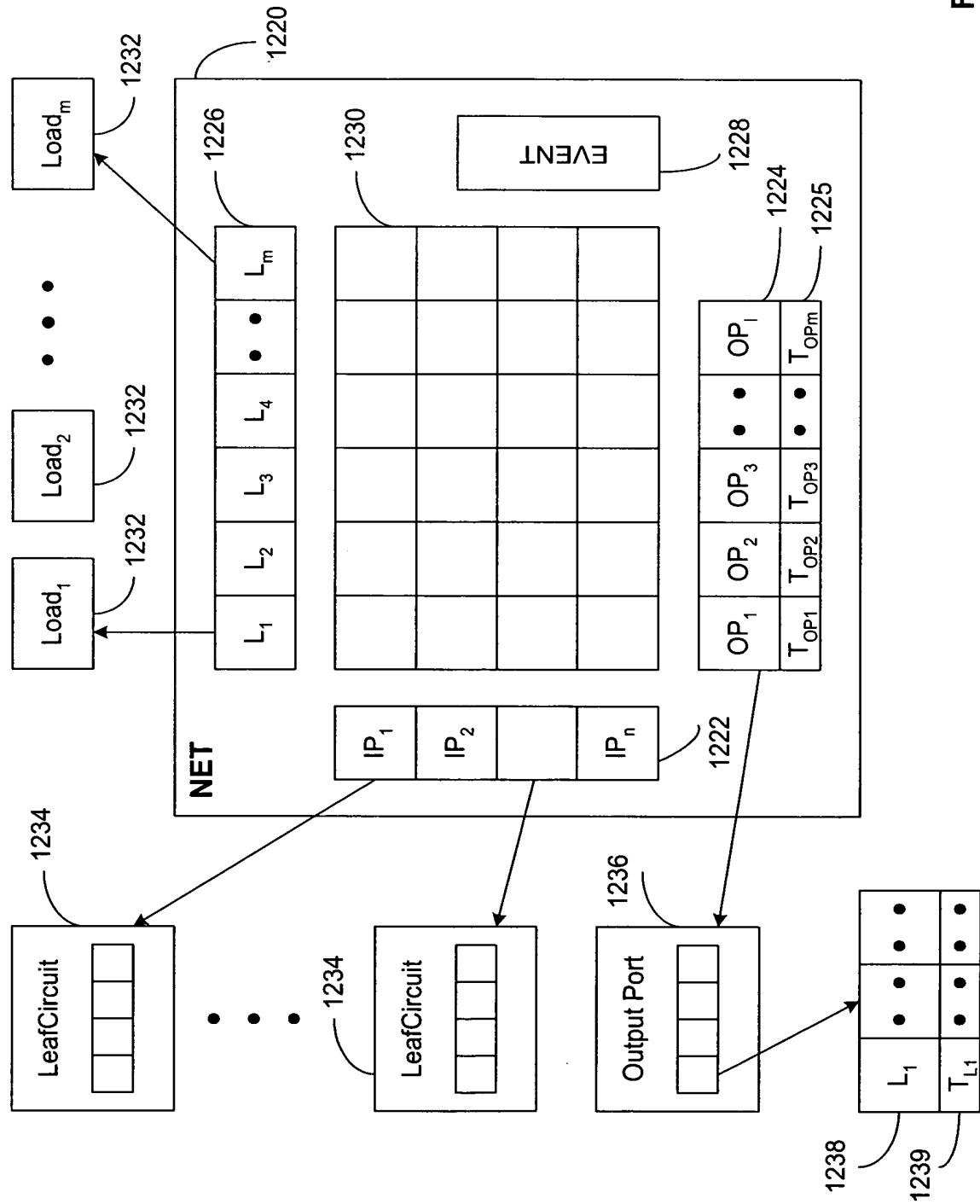


FIG. 12B

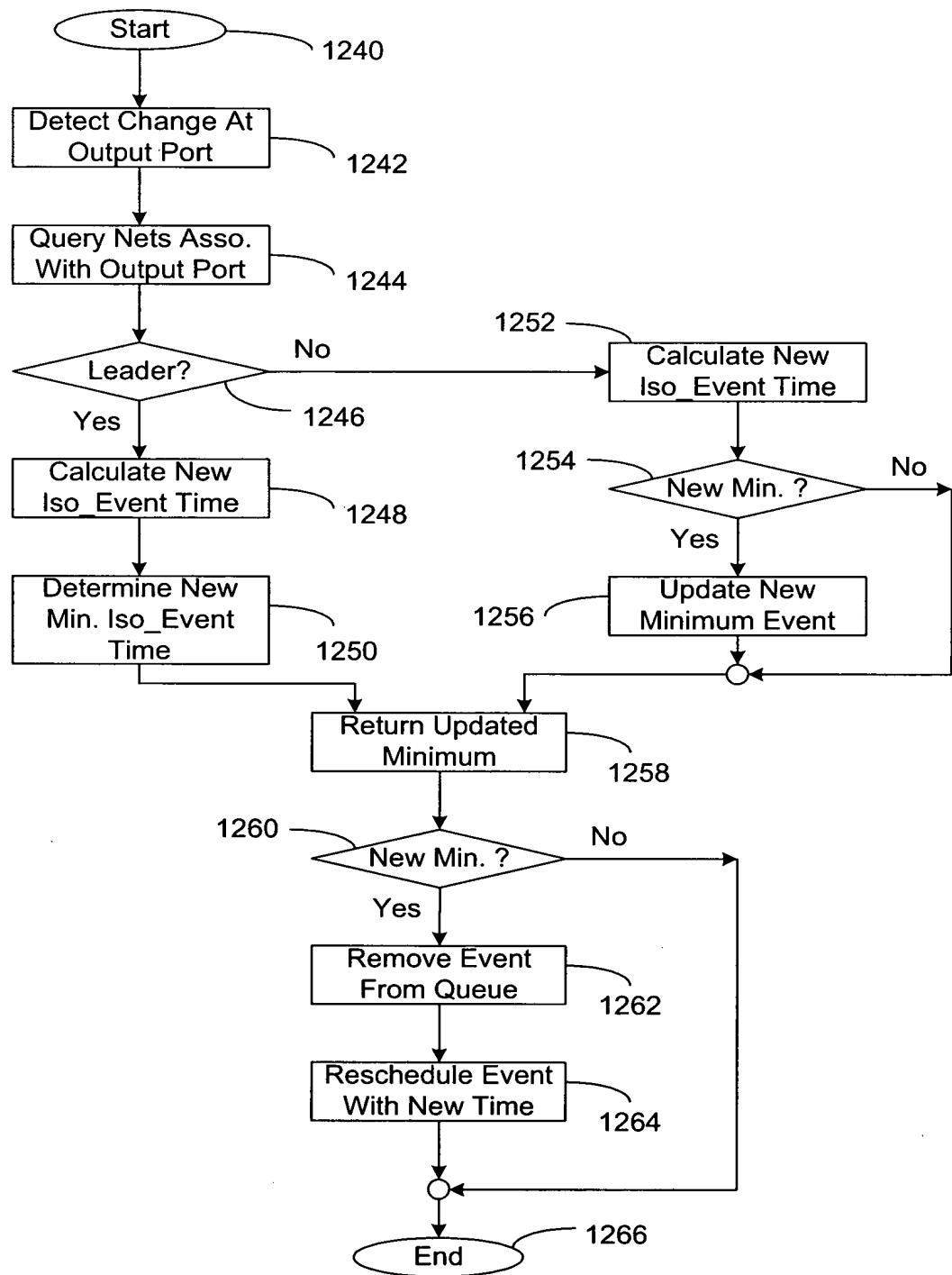


FIG. 12C

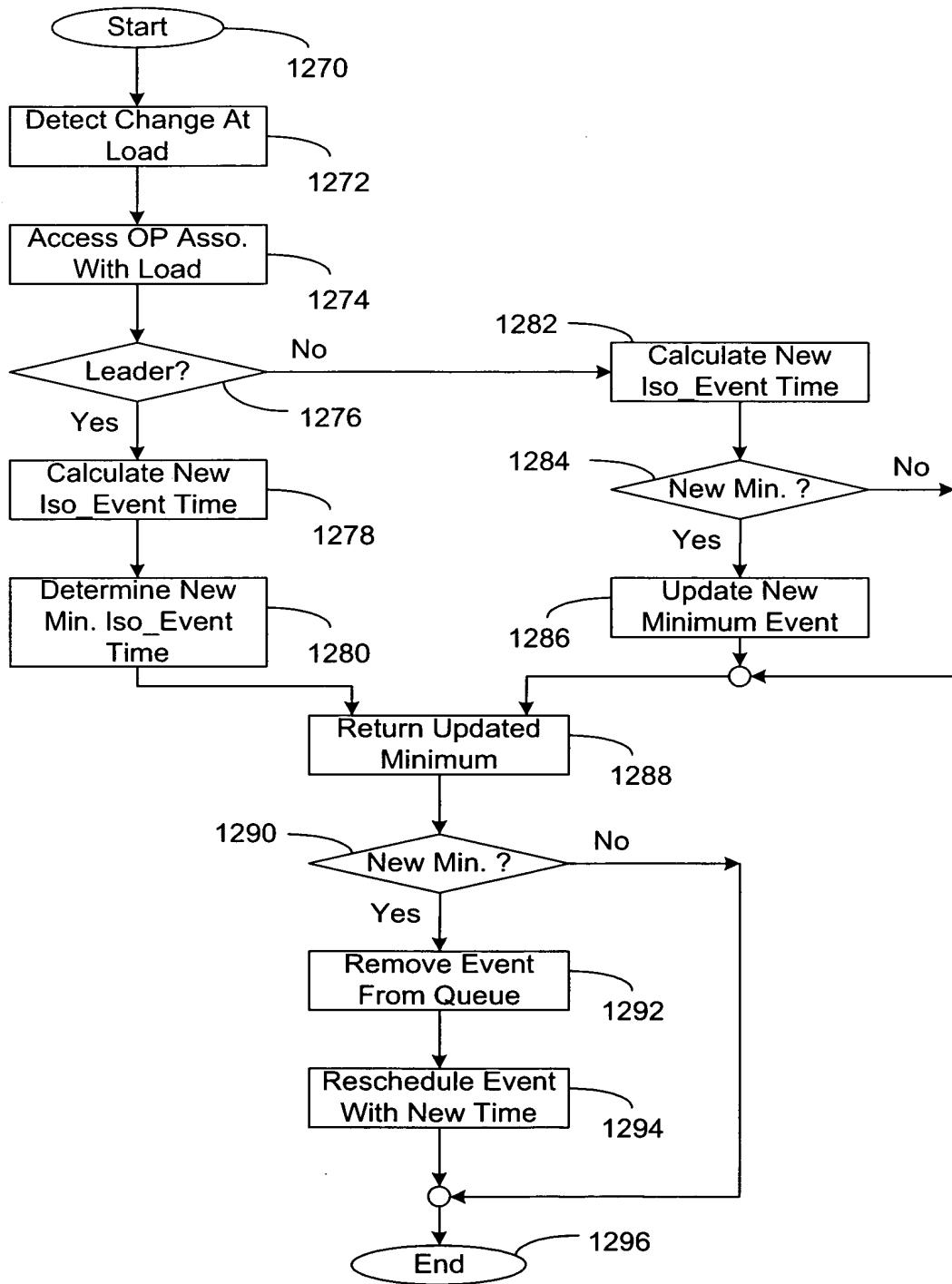


FIG. 12D

Event Diagram

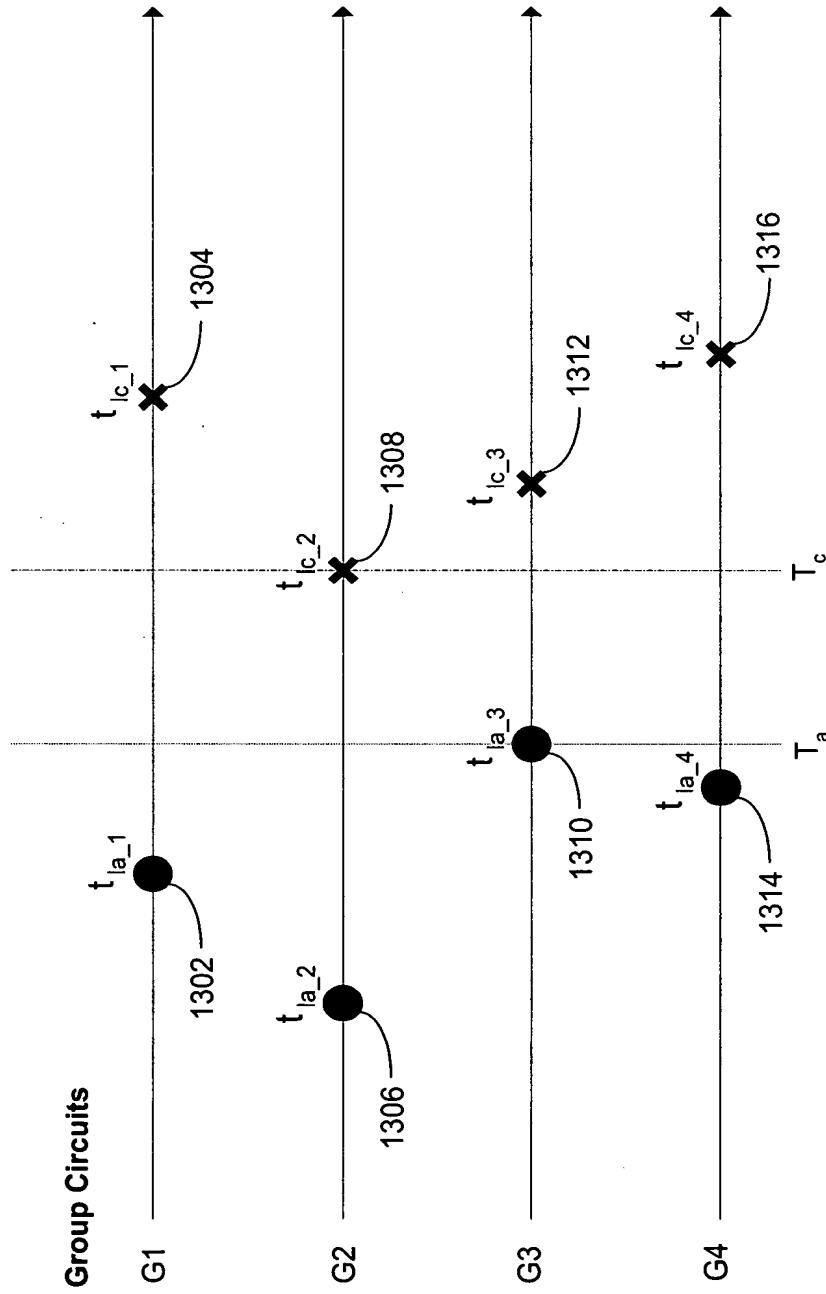


FIG. 13A

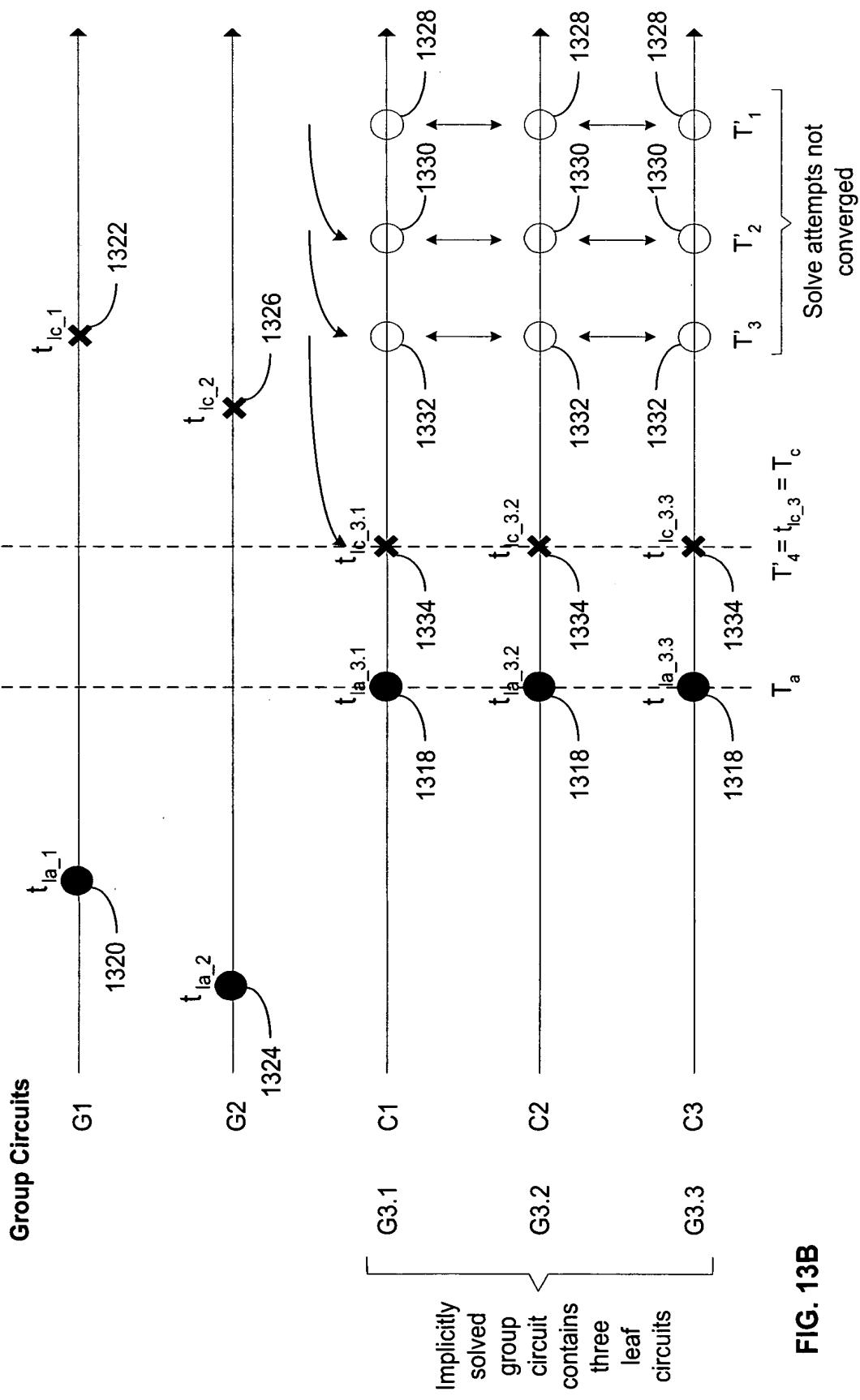


FIG. 13B

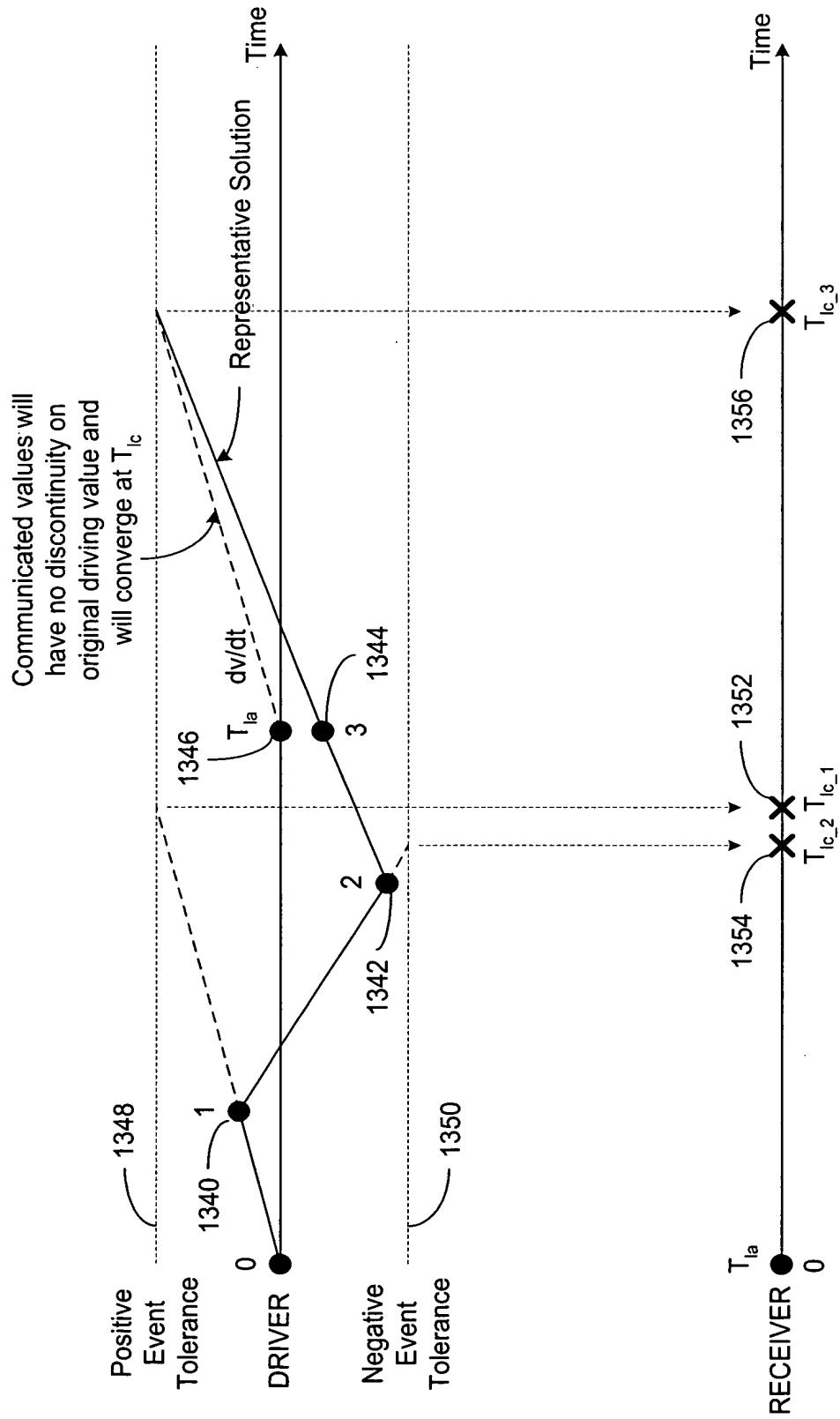


FIG. 13C

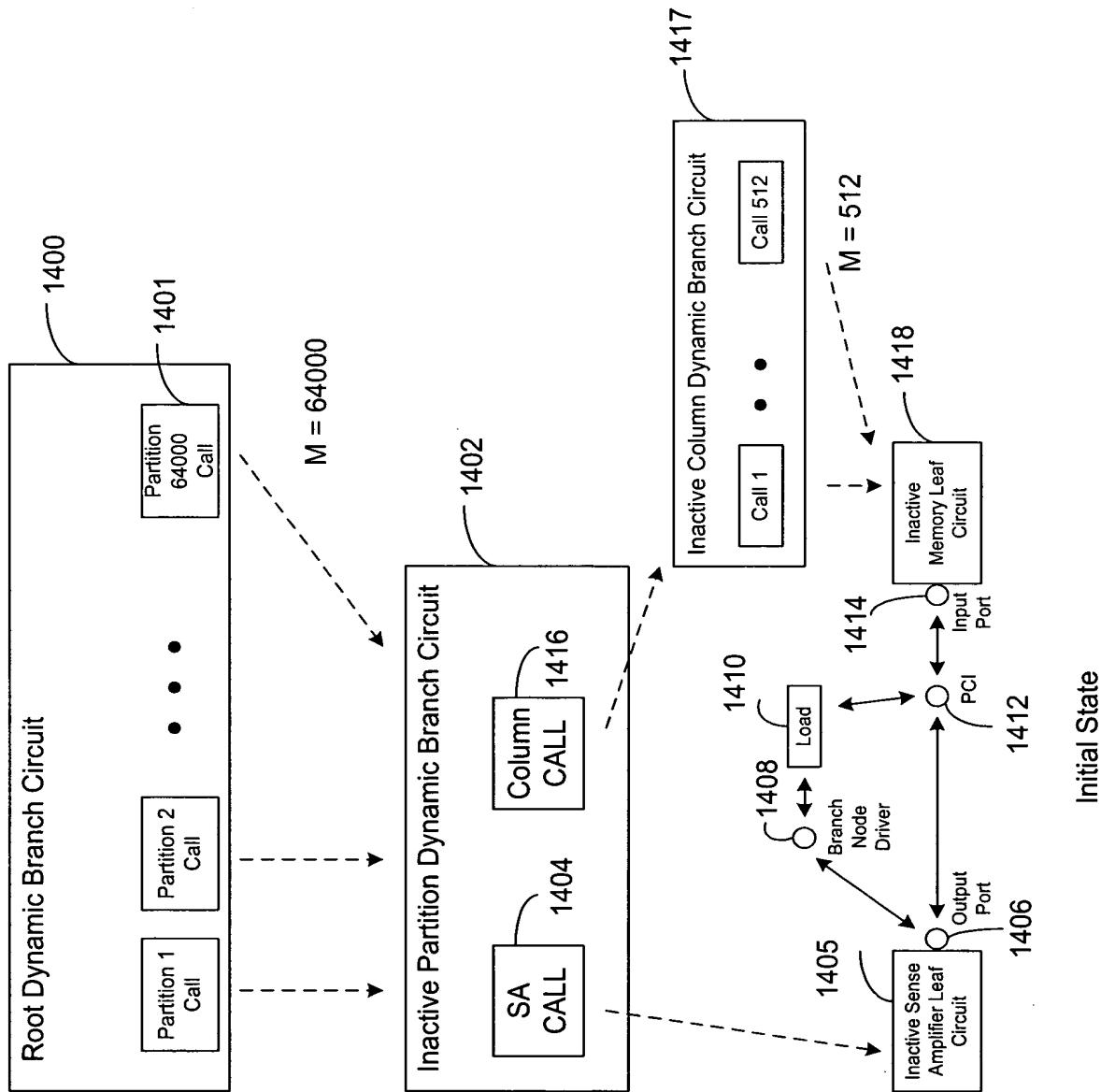


FIG. 14A

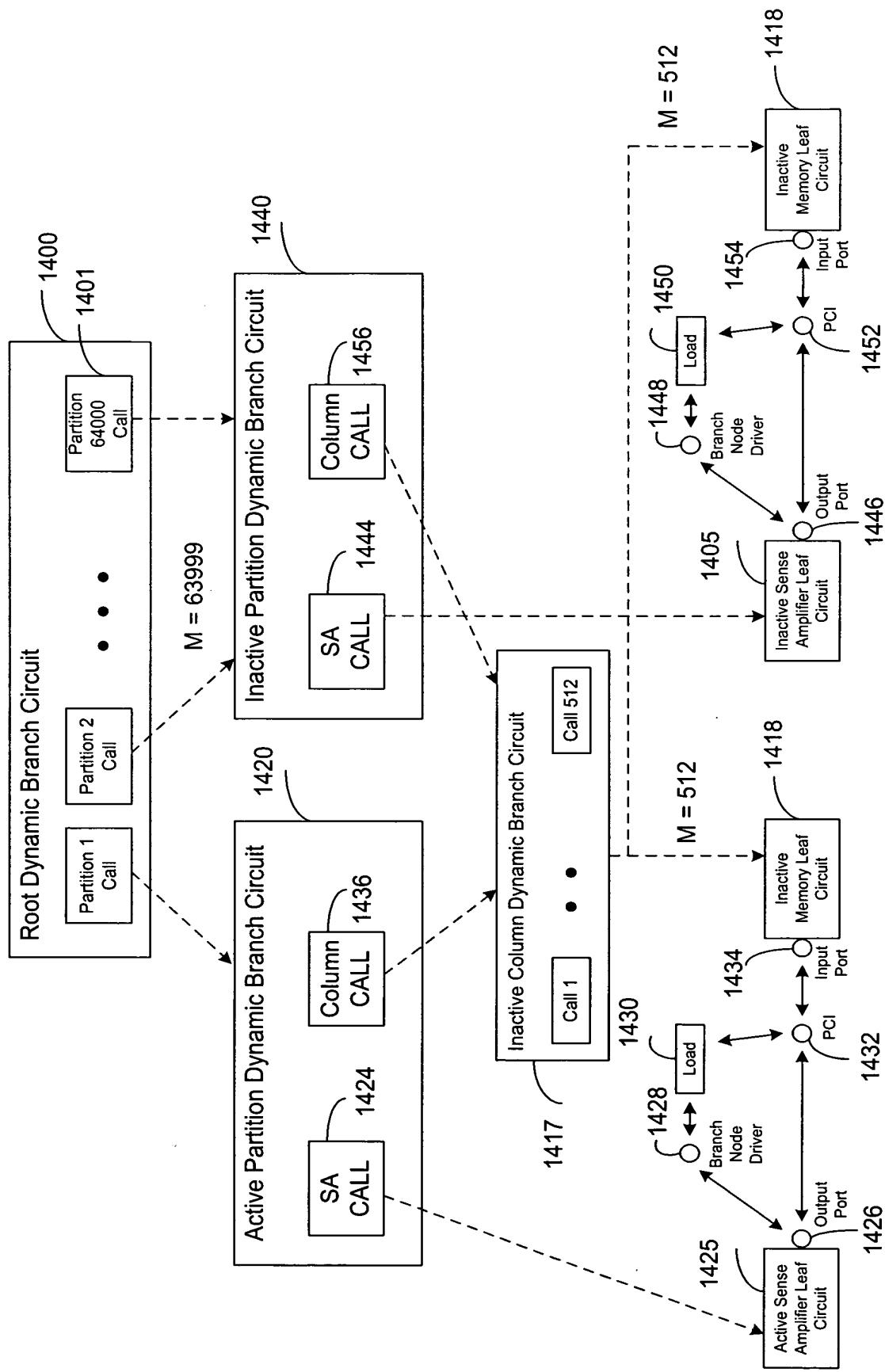


FIG. 14B

During Simulation When One Of The Sense Amplifiers Is Active And The Column Driven By The Sense Amplifier Is Inactive

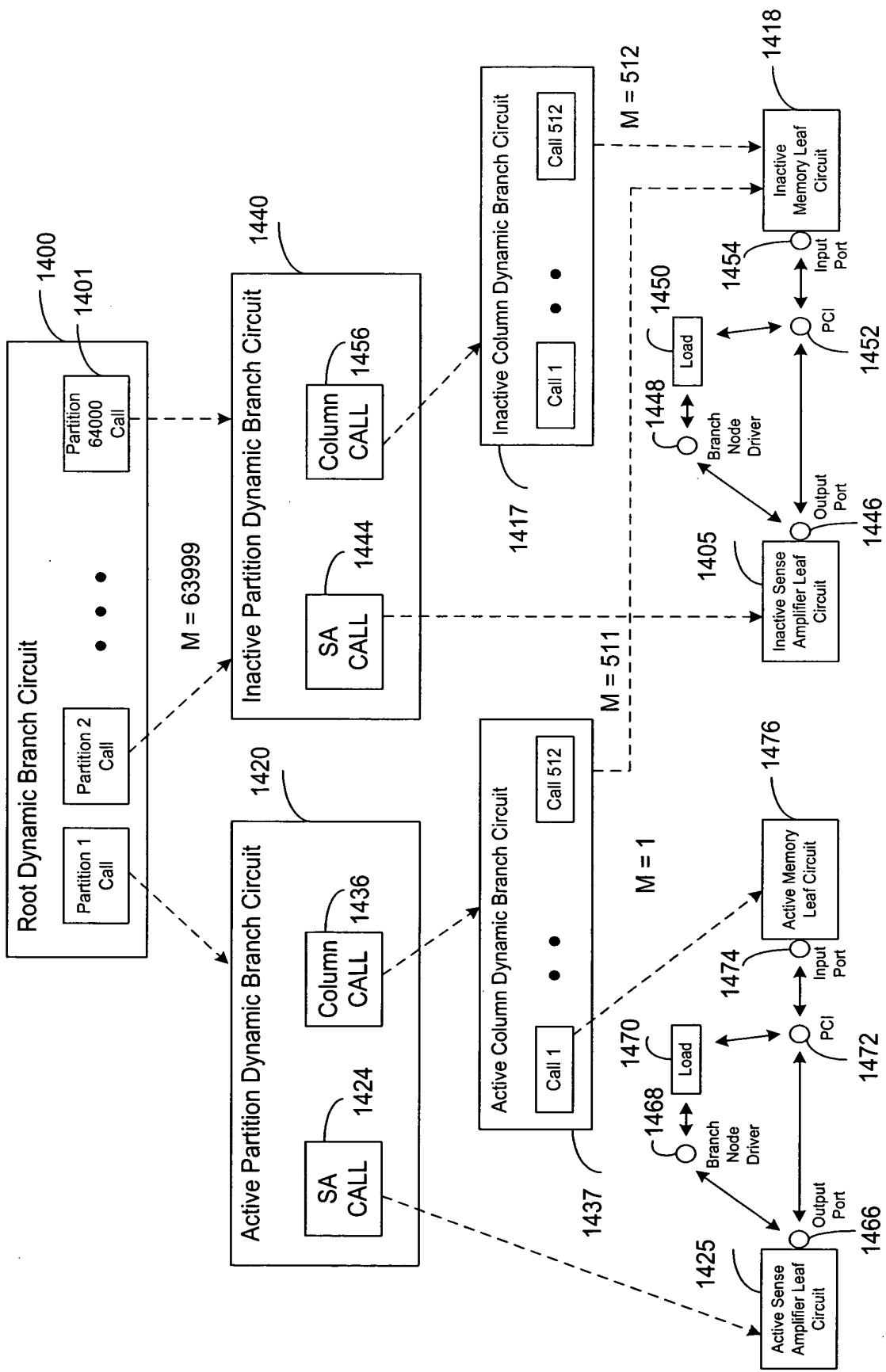


FIG. 14C During Simulation When One Of The Memory Leaf Circuits Driven By The Corresponding Active Sense Amplifier Is Active